REMARKS

Claim 14 has been editorially amended. The attachment to this Amendment entitled "Version with Markings to Show Changes Made" is a marked-up version of the changes made to the claims. The Applicant has carefully and thoughtfully considered the Office Action and the comments therein. For the reasons given below, it is submitted that this application is in condition for allowance.

1. In the Information Disclosure Statement filed April 5, 1999, a typographical error exists for the AQ entry in the Form PTO-1449 attached to the Information Disclosure Statement. For the AQ entry, the page numbers should be changed from "pp. 399-349" to --pp. 399-439--. The AQ document was submitted with the Information Disclosure Statement with pages 399-439. The Office Action mailed June 5, 2001 included an initialed copy of the Form PTO-1449, indicating that the AQ document was considered.

It is respectfully requested that the typographical error for the AQ entry be corrected. If an additional copy of the Form PTO-1449 and/or the AQ document is needed, please advise the undersigned, and it shall be provided in response thereto.

2. In the Office Action on pages 2-5 in section 2, claims 1-6 and 8-14 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,575,844 to Kosuge et al. (hereafter Kosuge). Applicant respectfully traverses this rejection.

The invention of the application teaches a switching mechanism where TDM and packet data are switched by a single shared memory mechanism such that switching packet data has no latency or jitter effect on the TDM traffic. See, e.g., specification, page 5, 14-24. TDM and

packet shared memory partitions and packet data queues per port contribute to the lack of latency or jitter effect on the TDM traffic. A varying amount of shared memory is used to store packet data, whereas the TDM portion of the shared memory is constant. Additionally, the use of routing information stored as part of a data exchange unit (DEU) assists in routing packet data. The switching of packet data by the shared memory has no latency or jitter effect on the switching of TDM data by the shared memory.

Claim 1 recites a switch for switching TDM data and packet data from input ports to output ports. The switch comprises a plurality of input ports, a plurality of output ports, and a shared memory. The plurality of input ports receives data, and each data comprises either TDM data or packet data. The plurality of output ports transmits switched data. The shared memory couples the input ports to the output ports and sequentially receives the data from the input ports. The shared memory switches a sequentially received data from a respective input port to a respective output port. The switching of packet data by the shared memory has no latency or jitter effect on switching of TDM data by the shared memory.

Kosuge teaches a digital switching system in Figure 1 having a hierarchical storage. The hierarchical storage includes a small-capacity high-speed memory 11, a large-capacity low-speed memory 12, and a file memory 13. For circuit switching, the high-speed memory 11 is used. Kosuge, column 3, lines 29-35; column 6, lines 4-8 and 15-18; Figures 4 and 5. For packet switching, the high-speed memory 11, the low-speed memory 12, and the file memory 13 are used. Kosuge, column 3, lines 29-39column 6, lines 8-14 and 18-25; Figures 4 and 5. Kosuge, however, fails to teach at least two aspects of claim 1.

First, Kosuge fails to teach a single shared memory to switch TDM data and packet data. Instead, Kosuge teaches using **three separate and distinct memories**, namely the high-speed

memory 11, the low-speed memory 12, and the file memory 13. Kosuge, Figure 1; column 3, lines 24-27; column 6, lines 8-25. The system of Kosuge requires **three** memories to implement the switching of both circuit data and packet data, whereas the claimed invention requires only a **single** shared memory to switch both TDM data and packet data. Hence, Kosuge fails to teach the recited shared memory.

Second, Kosuge fails to teach the avoidance of latency or jitter effects on the switching of TDM data by a shared memory due to the switching of packet data by the shared memory. Although Kosuge recognizes that packet data switching imparts non-constant delays in a switching system, Kosuge fails to recognize that jitter effects can also occur in such a system. Kosuge, column 6, lines 13-16. Additionally, the system of Kosuge is **not** described as minimizing latency effects and jitter effects on the switching of circuit data. Moreover, Kosuge fails to teach that **no** latency and jitter effects occur when switching circuit data by the shared memory due to the switching of packet data. Kosuge fails to appreciate the need to avoid the impact of packet processing on TDM latency or jitter and fails to disclose that switching of packet data by a shared memory has no latency or jitter effect on switching of TDM data by the shared memory.

Claims 2-9 and 14 are dependent from claim 1 and are allowable as being dependent from an allowable claim.

Further, claim 5 recites that the shared memory places sequentially received packet data in a queue for a respective output port. The use of queues for packet data and the ordered withdrawal of packet data from a queue are discussed in the application, for example, on page 11 at lines 10-13 and 20-23. In contrast, Kosuge teaches using **buffers** to store packet data. Kosuge, Figure 5, buffers in 12 and 13; column 6, lines 8-14 and 18-25. Kosuge fails to teach

the ordered withdrawal data from the buffers, as required for withdrawing data from a queue. Kosuge provides no explanation as to how data is input and output from the buffers. For example, Kosuge does not disclose whether or not the buffer includes header pointers and link lists, as can be used in a queue. Hence, Kosuge fails to teach a queue for packet data.

Claim 6 recites that the data received by the input and transmitted by the output ports are data exchange units. See, e.g., specification, page 5, line 5, to page 6, line 9. For packet data, the data exchange units can include header information. See, e.g., specification, page 12, lines 18-29. In contrast, Kosuge fails to mention or even refer to the concept of "exchange units" or "data exchange units." Instead, Kosuge teaches the usage of **time slots** on the input and output time division transmission lines 15 and 16. Kosuge, column 3, lines 31-32; column 5, line 63, to column 6, line 4; Figures 4 and 5. Additionally, Kosuge fails to teach the using control information **within the timeslot data itself** to control the writing of the data into and reading of the data out of the three memories 11, 12, and 13, as well as between the input ports and the output ports. The recited data exchange units are **not** the same as the timeslots of Kosuge. Hence, Kosuge fails to teach data exchange units.

Claim 10 recites subject matter similar to that recited in claim 1 and is allowable over Kosuge for the same reasons discussed above for claim 1.

Claims 11 and 12 are dependent from claim 10 and are allowable as being dependent from an allowable claim.

Further, claim 12 recites that the output port to which TDM data is routed is determined based on a time slot in a frame in which the TDM data was received by the input port, and that the output port to which the packet data is routed is determined based on routing data embedded in the packet data and based on the input port which received the packet data. The use of routing

data embedded in the packet data is discussed in the specification, for example, on page 12 at lines 18-22. In contrast, Kosuge teaches using a **separate** time division multiplex control channel to direct the switching based on the time slot that the data arrives on the input port. Kosuge, column 6, lines 61 ff; Figure 3, blocks 100, 101, and 102; Figure 6, blocks 17R, 401, 402, 408, 404, and 403. Using the control channel to direct switching as in Kosuge is **not** the same as embedding routing information in the packet data as in the recited invention. Hence, Kosuge fails to teach the routing of packet data as recited.

Claim 13 recites subject matter similar to that recited in claim 1 and is allowable over Kosuge for the same reasons discussed above for claim 1.

Claim 14 recites that data is received by the input ports and transmitted by the output ports as data exchange units. The data exchange units are packet data comprising routing information. Switching of a data exchange unit from a respective input port to a respective output port is controlled by a stored switch configuration. The stored switch configuration uses the routing information of data exchange units for packet data to determine respective output ports to switch the data exchange units. As discussed above for claims 6 and 12, Kosuge fails to teach using data exchange units and using routing data embedded in the packet data. For the same reasons discussed above for claims 6 and 12, Kosuge fails to teach the limitations recited in claim 14.

3. In the Office Action on page 5 in section 4, claim 7 is objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form. The Applicant thanks the Examiner for the indication of allowable subject matter. Because claim 7 is dependent from claim 1, which is allowable as discussed above, the Applicant whishes to defer

placing this claim in independent form at this time and respectfully requests that this claim be allowed.

4. Claim 14 has been amended to correct a typographical error and not avoid or overcome any rejections.

THEREFORE, because all rejections have been overcome, it is submitted that claims 1-14 are allowable, and such allowance is requested.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 14 is amended as follows:

--14. (Amended) A switch as claimed in claim 1, wherein the data are received by said input ports and transmitted by said output ports as data exchange units, the data exchange units for packet data comprise routing information, the switching of a data exchange unit from a respective input port to a [respect] respective output port is controlled by a stored switch configuration, said stored switch configuration uses the routing information of data exchange units for packet data to determine respective output ports to switch the data exchange units.--